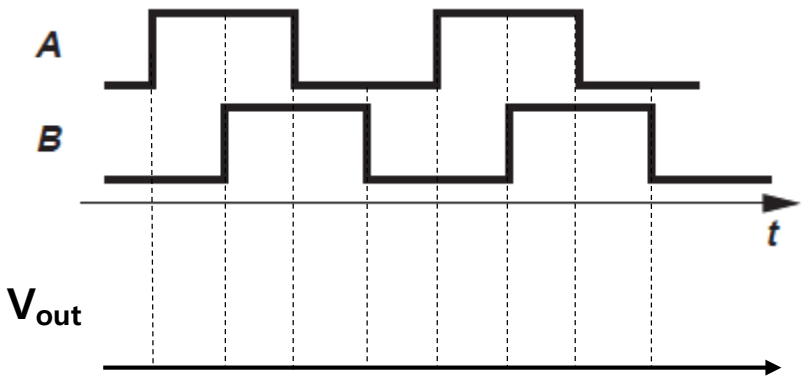
EE304 Microelectronics Homework 4

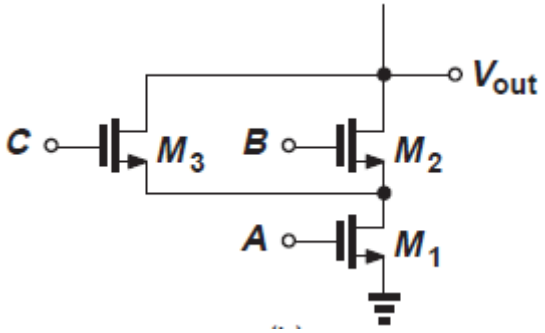
Due date: 13:00, 15th, December

Solve problems below.

#1. A CMOS NAND gate drives a load capacitance of 20fF. Suppose the input waveforms are as shown below, each having a frequency of f_1 = 500 MHz. Draw the output waveform and calculate the power dissipated by the gate. Neglect the crowbar current. [20 Points]

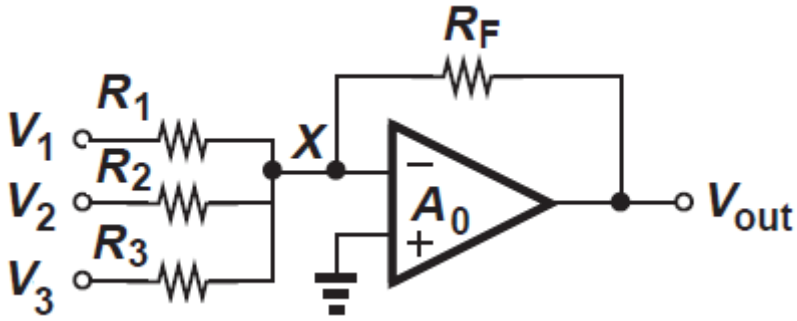


#2. For NMOS shown below, draw the dual PMOS section, construct the overall CMOS gate, and determine the logical function performed by the gate. [20 Points]



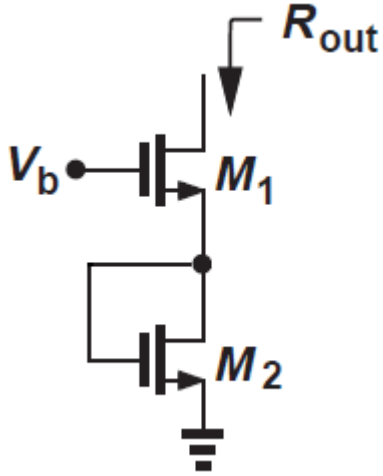
#3. For below figure, if $V_1 = 0.8V$, $V_2 = 1.1$ and $V_3 = 0.5V$. $R_1 = R_2 = R_3 = 5k\Omega$ and $R_F = 10k\Omega$ $A_0 = \infty$, find V_{out}. The notation at the positive terminal of the operational amplifier is the symbol for ground or 0V.

[20 Points]



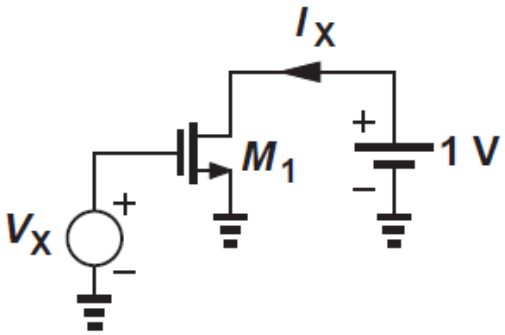
#4. For the circuit shown below, CS stage with degeneration (MOS connected load), find R_{out} using equivalent circuit.

[20 Points]

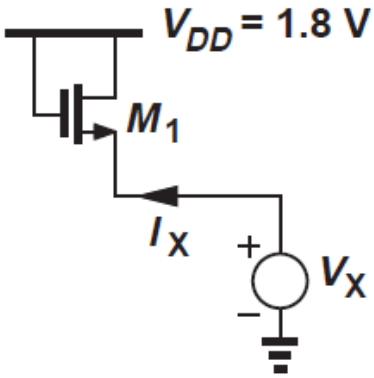


#5. Sketch I_X as a function of V_X for the circuits (a) and (b) shown below. Assume V_X goes from 0 to V_{DD} = 1.8V and V_{TH} = 0.4V. Also, λ = 0. Determine at what value of the device changes its region of operation. Specify operating regions on your I-V graph.

[20 Points]



(a)



(b)

NOTE

- If you drive answer without sufficient explanation, your score will not be given fully.

- There is final exam 15th, December. Therefore, you should submit your homework4 just before the final exam begins. Of course, submitting late is NOT acceptable.

- You should write all your answers in English.