Real-Time Per-Cycle Energy Consumption Measurement of Digital Systems

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This technical report introduces a real-time per-clock-cycle energy measurement technique for power analysis and reduction of synchronous state machines. This technique guarantees accuracy with a sampling rate of twice the clock frequency under spiky current draw common in digital systems. In addition, it acquires the energy consumption profile in real-time, thus, not requiring repeated operation of the target system.

Introduction: Range of power reduction techniques are introduced as power consumption emerges from other performance metrics. The first step of the power reduction is power estimation and/or measurement. Simulation-based power estimation [1, 2] is convenient only in so far as a model is available. Empirical approaches do not rely on a model, but accurate measurement is usually difficult.

Power measurement is conventionally performed by standard equipment. However, there are often limitations inherent in traditional methodologies. For example, digital multimeters [3] restrict the measurement to the average power consumption under repeated execution of the target system due to a slow response time. Digital oscilloscopes are able to achieve high-sampling rates [4], but are invariably error-prone because of the current spikes common in digital systems.

This report, therefore, introduces a real-time per-cycle energy consumption measurement so as to accomplish fast and accurate power analyses. The principle of operation is based on charge transfer enabling the system to measure exact energy consumption without a high-sampling rate. It is robust to the current spikes as well. The real-time acquisition capability does not require repeated operation of the target system as in previous empirical methods. PC Windows-based software supervises the measurement hardware and exchanges the energy profile with other applications for easy analysis.

Principle of operation: This report assumes that the target technology is rail-to-rail CMOS, and there is no asynchronous input signal. The first assumption is widely accepted for on-chip circuits and allows for counting solely in dynamic power. The second assumption is generally accepted because asynchronous input signals are usually synchronized to the system clock. There is no further energy consumption when the state machine stabilizes in each clock cycle.

The i-th-cycle energy consumption of a synchronous finite state machine, Δq_i, is defined by the amount of the charge transfer:

$$\Delta q_i = \frac{C_s v_{s-}^2(i)}{2} - \frac{C_s v_{s+}^2(i)}{2} \tag{1}$$

Figure 1

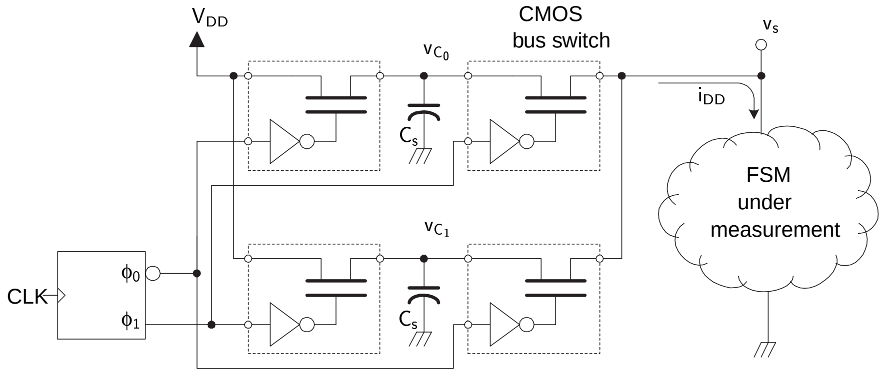

Figure 1: Measurement circuit using switched capacitors

where $v_{s-}(i)$ and $v_{s+}(i)$ are the initial and the final voltages of v_s in the i-th clock period, respectively. C_s is the reference capacitor as shown in Fig. 1. Power consumption of the i-th clock period, Φ_i, is given by $\Phi_i = f\Delta q_i$. The average power, Φ, is then $\Phi = \frac{1}{f}\sum \Delta q_i$.

The measurement circuit (Fig. 1) consists of low-resistance fast FET switches and high-frequency capacitors. The supply voltage, v_s, is measured by a level-shifter and a fast A/D converter. The capacitor charges for one clock and discharges for another. Fig. 2 illustrates conceptual waveforms. The supply voltage, v_s, should remain in the operating range of the circuit under test.

Measurement system: High performance CMOS bus switches (e.g., FST3125) have a few ns switching time and several Ω on-resistance; lower on-resistance is achieved by parallel connections. The value of v_s is converted by a differential input pipelined A/D converter (e.g., OPA681). The system stores the energy consumption profile in a high-speed SRAM in real-time. An FPGA vector generator minimizes the interference added by the measurement process. For instance, it allows a microprocessor to execute repeatedly without adding jump or loop instructions. The I/O buffers consume much more power on orders of magnitude than on-chip bus buffers. Therefore, it is important to avoid power measurement under differently loaded external buses.

Comparison with voltage measurement: Amperemeters measure voltage drop across the series resistor inserted to the power supply line. So, measurement of current is equivalent to the measurement of voltage. The power supply current of synchronous state machines dynamically changes in a very short period. Due to the limited bandwidth of the voltmeters, a low-pass filter such as a bypass capacitor should be attached to the power supply trace. The voltmeter is, therefore, only able to measure the average power consumption. High-bandwidth digital oscilloscopes, on the other hand, can capture the voltage envelope. It is error-prone in acquiring the voltage envelope, and thus, the energy consumption, because the power spectrum is usually significant up to hundreds of MHz (Fig. 2 (a)).

We can measure the exact amount of the charge transfer, in contrast, by sampling the supply voltage, v_s, only two times in a clock period. It is quite affordable to build a customized data acquisition system in the field with COTS (commercial off-the-shelf) components for automatic measurement. It dramatically reduces the amount of data with comparable accuracy to the voltage measurement. The value

Figure 2

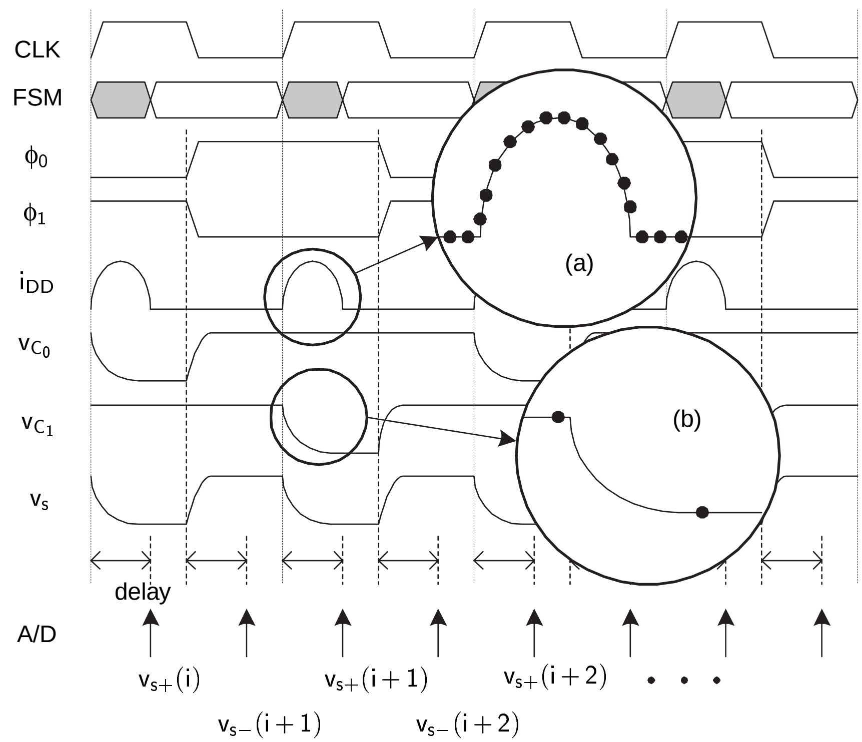

Figure 2: Waveforms of the clock-cycle-level energy consumption measurement system ((a): sample points for voltage measurement and (b): sample points for the proposed method)

Figure 3

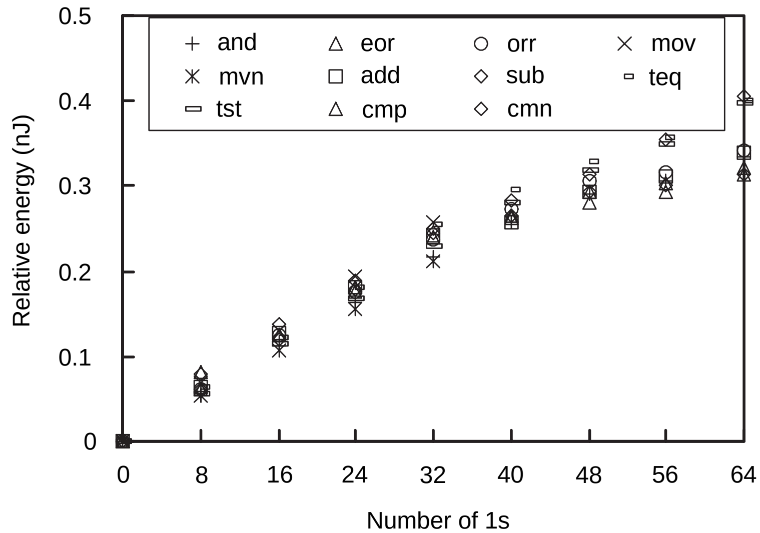

Figure 3: Energy consumption of the ARM7TDMI core by the operand values (EX stage)

of v_s during the transient state does not affect the measurement process; only the initial and the final voltages are meaningful: v_{s-} and v_{s+}. It is easier to eliminate the noise because the supply voltage, v_s, always remains in a steady state as the A/D converter samples it (Fig. 2 (b)).

Experimental results: The accuracy of the proposed method is demonstrated by a CMOS 4-bit binary counter, 74HC393. We first measured the average power supply current with a multimeter: 1.68mW (@ 5MHz) and 3.39mW (@10MHz). We measured the per-cycle energy consumption by the proposed method ($C_s = 3,200pF$). The 74HC393 consumes 0.21nJ, 0.35nJ, 0.49nJ, and 0.62nJ when the numbers of the output changed are 1, 2, 3, and 4 bits, respectively. The equivalent average power consumption was found to be 1.64mW (@5MHz) and 3.26mW (@10MHz).

We also demonstrate that the method is applicable to complex state machines with the ARM7TDMI RISC processor. Due to limited space, this report summarizes only a part of the results. Fig. 3 shows the energy variation of the EX stage by the register values over 11 instructions. It shows that the energy consumption is proportional to the number of 1's in the operand regardless of the opcode. This is explained by the dynamic CMOS configuration of the ARM7TDMI core.

Conclusion: The proposed energy measurement method is fast, efficient and accurate. It guarantees accuracy with a sampling rate of twice the clock frequency, and thus makes it possible to build the system with low-cost COTS components. It is able to take a snapshot of the energy profile without disturbing the target system. This capability is very important in performing diverse experiments indispensable in energy characterization of complex digital systems. The measurement system plays an important role in system-level power analysis and low-power software research.

References

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